IN THE SPECIFICATION

In the Specification:

Please replace paragraph [0010] on page 3 with the following rewritten paragraph:

[0010] The sequencers control the application of the operations in accordance with the timing characteristics of their respective memory modules. For example, each of the sequencers controls the application speed of the sequence of operations in accordance with the access speed of the respective memory module. A single sequencer may control the application of the test algorithms to a plurality of memory modules that operate on a common clock domain. Consequently, logic for controlling application timing and sequencing of the test pattern domain is incorporated within the sequencers, and need not be distributed within the individual memory modules or maintained by the BIST controller.